Agilent Technologies
81100 Family of
Pulse Pattern Generators

Technical Specifications

Agilent 81110A

Signals for testing digital designs and components

The Agilent 81101A, 81104A, 81110A and 81130A generate all the standard pulses and digital patterns needed to test current logic technologies (CMOS, TTL, LVDS, ECL, etc.).

With the optional second channel on all of the models from 80 MHz to 660 MHz, multi-level and multi-timing signals can be obtained using the internal channel addition feature.
- Variable pulse parameters in pattern mode as well as in pulse mode (not on the 81130A)
- Synchronously triggerable
- Simulation of reflections/distortions (81104A, 81110A)
- Three/four-level codes (81104A, 81110A)

Flexible pulses or patterns for digital designs

Key Features

- Pattern mode on all models from 80 MHz to 660 MHz, including pseudo-random binary sequence.
- The outputs of dual-channel instruments can be added (analog or EXOR, depending on model).
- User-retrofittable channels for most models
- Upward compatibility
- Individual solutions for frequencies up to 50, 80, 165, 330, 400 and 660 MHz
- 100% form/fit compatibility

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Glitch-free timing changes

Timing values can now be swept without the danger of misleading pulses or dropouts that could cause measurement errors. (Applies to continuous mode, values < 100 ms, consecutive values between 0.5 and twice the previous value on the 81101A, 81104A, 81110A)

Reliable measurements

All models provide clean, accurate pulses with excellent repeatability, thus contributing to measurement integrity.

The Agilent 81110A features self-calibration for more accuracy. It also offers a choice of output modules. The Agilent 81111A 165 MHz 10 V module with variable transitions. Along with the Agilent 81112A 330 MHz 3.8 V module,

which has differential outputs and two selectable transition times. The Agilent 81130A offers a choice of output modules: the Agilent 81131A 400 MHz, 3.8 V module and the Agilent 81132A 660 MHz, 2.5 V module which has complementary outputs.

Easy-to-use

Features such as the clear graphical display, autoset, help, store/recall, preset TTL/ECL levels, selectable units (such as current/voltage, width/duty-cycle), and load compensation ensure a high level of convenience.

Stimulate the device's environment

Today's devices can require very complex stimuli. To meet this, the Agilent 81130A can sequence and loop its memory for very deep patterns. RZ (return-to-zero), NRZ (non-return-to- zero) and R1 (return-to-one) formats are available. Digital channel addition allows the generation of signals with two different pulse widths and delays or of data rates up to 1.32 Gbit/s in one single channel.

Frequency range

The Agilent 81130A is designed and recommended for an operation in the frequency range of 170 kHz to 400/660 MHz. However it can be operated in the extended range down to 1 kHz.

Agilent 81100 - Family of Pulse Pattern Generators

Mainframes	81101A	81104A	81110A3		81130A	
Channel Model	n.a.	81105A	81111A	81112A	81131A	81132A
Nr. of channels	1	1 or 2	1 or 2		1 or 2	
	Single ended	Single ended	Single ended	differential	Single ended	differential
Frequency range	1 mHz - 50 MHz	1 mHz - 80 MHz	1 mHz - 165 MHz	1 mHz - 330 MHz	1 kHz - 400 MHz	1 kHz - 660 MHz
Period range	20 ns to 999.5 s	12.5 ns to 999.5 s	6.06 ns to 999.5 s	1.515 ns to 999.5	2.5 ns to 1 ms	1.5 ns to 1 ms
Variable delay range	0.00 s - 999.5 s	0.00 ns - 999.5 s	0.00 ns - 999.5 s		0.00 ns to 3.00 μs	
Period RMS - jitter	0.01% + 15 ps^2	0.01% + 15 ps^2	0.01% + 15 ps^2		0.01% + 15 ps^2	
Width range	10 ns to 999.5 s	6.25 ns to 999.5 s	3.03 ns to 999.5 s	1.515 ns to 999.5 s	1.25 ns to (period-1.25 ns)	70 ps to (period-750 ps)
Amplitude range	100 mV to 20.0 V^1	100 mV to 20.0 V^1	100 mV to 20.0 V^1	100 mV to 3.8 V	100 mV to 3.8 V	100 mV to 2.5 V
Transition time range (10/90)	5.00 ns to 200 ms	3.00 ns to 200 ms	2.00 ns to 200 ms	800 ps or 1.6 ns selectable	800 ps or 1.6 ns selectable	500 ps typ. fixed
Dropout- and glitch- free timing change	yes	yes	yes		No	
Source Impedance	50 Ω or 1 kΩ	50 Ω or 1 kΩ	50 Ω or 11 kΩ	50 Ω	50 Ω	

(1)   **Depends on selected impedance (all other values for 50 Ω source impedance into 50 Ω load)**
(2)   **0.001% +15 ps with internal PLL as clock source**
(3)   **Also avalable as VXI Pulse Pattern Gernerators E8311A and E8312A**

81101A Specifications

Timing Characteristics

Measured at 50% amplitude at fastest transitions in continuous mode and 50 Ω source impedance.

Mainframe	Agilent 81101A
Frequency range	1mHz to 50MHz
Timing resolution	3.5 digits, 5ps best case
Period RMS jitter	
With PLL	0.001% + 15 ps
With VCO	0.01% + 15 ps
Period range	20ns to 999.5 s
Accuracy with PLL /VCO	± 0.01% (±5%) (similar to RMS Jitter)
Width range	10.0 ns to (period - 10.0 ns)
Accuracy	±5% ±250 ps [1]
RMS Jitter	0.01% + 15 ps
Additional variable delay range	0 ns to (period -20 ns)
Accuracy [2]	±5% ±1 ns
RMS Jitter	0.01% + 15 ps
Double pulse delay range	(width + 10.0 ns) to (period- width - 10.0 ns)
Accuracy	±5% ± 500 ps
Transition time range (10/90)	5 ns to 200 ms variable
Accuracy	±10% ±200 ps
Linearity	3% typ. for transitions > 100 ns

Note:
(1) Changing of amplitude may add 0.5 ns.
(2) Width accuracy specification is valid up to 5.5 Vpp amplitude. Above this amplitude, the width will typically increase up to 300ps

Burst Count: 2 to 65536 (single or double pulses).

Delay: Delay, phase or % of period.

Double pulse delay: Double pulse and delay are mutually exclusive.

Duty cycle: Set between 0.1% and 95% (subject to width limits. 99.9% with overprogramming).

Transition times: These can be Entered as leading/ trailing edge or % of width. Leading and trailing edges are independent within one of the following overlapping segments (1:20 ratio):
5 ns - 20 ns, 10 ns - 200 ns, 100 ns - 2 µs, 1µs - 20 µs, 10 µs - 200 µs, 100 µs - 2 ms, 1 ms - 20 ms, 10 ms - 200 ms.

Transition times: These can be entered as leading/ trailing edge or % of width. Leading and trailing edges are independent within one of the following overlapping segments (1:20 ratio):
5 ns - 20 ns, 10 ns - 200 ns, 100 ns - 2 µs, 1µs - 20 µs, 10 µs - 200 µs, 100 µs - 2 ms,
1 ms - 20 ms, 10 ms - 200 ms.

Repeatability: Is typically four times better than accuracy

Output timing fidelity: Period, delay and width are continuously variable without any output glitches or dropouts.

Level/Pulse Performance Characteristics

Level specifications are valid after a 30 ns typical settling time.

		Agilent 81101A
Amplitude	50 Ω into 50 Ω	100 mV$_{pp}$ to 10.0 V$_{pp}$
	1 kΩ into 50 Ω	200 mV$_{pp}$ to 20.0 V$_{pp}$
Level window	50 Ω into 50 Ω	-10.0 V to +10.0 V
	1 kΩ into 50 Ω	-20.0 V to +20.0 V
Accuracy	50 Ω into 50 Ω	± (3% + 75 mV)
	1 kΩ into 50 Ω	± (3% + 150 mV) [1]
Resolution	50 Ω into 50 Ω	10 mV
	1 kΩ into 50 Ω	20 mV
Output connectors		BNC single-ended
Source Impedance		Selectable 50 Ω or 1 kΩ
Accuracy		Typ. ± 1%
Max. external voltage		± 24 V
Short circuit current		± 400 mA max.
Base line noise		10 mV RMS typ.
Overshoot/preshoot/ringing		± 5% of amplitude ± 20 mV

Note: (1) In ±19 V level window

Trigger Modes

Continuous: Continuous pulses, double pulses or bursts (single or double pulses).

External triggered: Each active input transition (rising, falling or both) generates a single or double pulse or burst.

External gated: The active input level (high or low) enables pulses, double pulses or bursts. The last single / double pulse or burst is always completed.

External width: The pulse shape can be recovered whilst the period and width of an external input signal are maintained. Levels and transitions can be set.

Manual: Simulates an external input signal.

Internal triggered: Internal PLL replaces an external trigger source.

Inputs and Outputs

Clock input/PLL reference and

external input: One input (BNC connector at rear panel) is used for clock input or alternatively for the PLL.

PLL Reference: The internal PLL is locked to an external 5 MHz or 10 MHz reference frequency.

Clock input: The output period is determined by the signal at CLK input.

Ext. input: Used for trigger, gate or external width.

Level parameters: Can be entered as voltage or current, as high and low level, or as offset and amplitude.

Load compensation: The actual load value can be entered (for loads ≠50 Ω) to display actual output values.

On/off: Relays connect/disconnect output (HiZ).

Normal/complement: Selectable.
Limit: Programmable high and low levels can be limited to protect the device-under-test.

Input impedance: 50 Ω/10 kΩ selectable.

Threshold: -10 V to +10 V.

Max. input voltage: ±15 Vpp.

Sensitivity: 300 mVpp typical.

Input transitions: <100 ns.

Frequency: Dc to 50 MHz .

Minimum pulsewidth: 10 ns

**Strobe output and trigger output
Trigger format:** One pulse per period with 50% duty cycle typical.

External mode: 9 ns typ.

Level: TTL or ECL selectable.

Output impedance: 50 Ω typical.

Max. external voltage: -2 V/+7 V.
Transition times: 1.0 ns typical for TTL, 600 ps typical for ECL.

Typical delay times Agilent 81101A

Instrument mode	From	To	Typ. value
External width	Ext. Input	Strobe/Trigger out	8.5 ns
		Output 1/Output 2	22.5 ns
All other modes	Ext. Input/Clk input	Strobe/Trigger out	12.0 ns
		Output 1/Output 2	29 ns
	Strobe/Trigger out	Output 1/Output 2	17 ns

81104A and 81110A Specifications

Timing Characteristics

Measured at 50% amplitude at fastest transitions in continuous mode and 50 Ω source impedance.

Mainframe	Agilent 81104A	Agilent 81110A	Agilent 81110A
Output module	**Agilent 81105A**	**Agilent 81111A**	**Agilent 81112A**
Frequency range	1 mHz to 80 MHz	1 mHz to 165 MHz	1 mHz to 330 MHz
From 1 KΩ	Up to 50 MHz typ.	Up to 60 Mhz typ.	N/A
Timing Resolution	3.5 digits, 5 ps best case		
Period Range	12.5 ns to 999.5 s		
Period RMS jitter			
With PLL	0.001% + 15 ps		
With VCO	0.01% + 15 ps		
Accuracy with			
PLL	0.001% +15 ps	± 0.01%	
VCO	± 0.01% (± 5%)	(± 0.5% typ. After self-cal., ± 3% without self-cal.)	
Width range	6.25 ns to (period 6.25 ns)	3.03 ns to (period - 3.03 ns)	1.515 ns to (period - 1.515 ns)
Accuracy	± 5% ± 250 ps	± 0.5% ± 250 ps typ. After self-cal. ±3% ± 250 ps	
Jitter (RMS)	0.01% + 15 ps		
Add. Variable delay range	0 ns to (period -12.5)	0 ns to (period -3.03 ns)	
Accuracy	± 5% ± 0.5 ns	± 0.5% ± 0.5 ns typ. ± 3% ± 0.5 ns after self-cal.	
Jitter (RMS)	0.01% +15 ps		
Double pulse delay range	12.5 ns to (period - width - 6.25 ns)	6.06 ns to (period - width - 3.03 ns)	3.03 ns to (period - width - 1.5) 6.06 ns (165 MHz) typ.
Min period	25 ns (40 MHz) typ.	12.2 ns (82 MHz) typ.	±0.5% ± 150 ps typ. ± 3%
			± 150 ps after self-cal.
Accuracy	± 5% ± 250 ps	±0.5% ± 150 ps typ. ± 3% ± 150 ps after self-cal.	
Transition time range (10/90)	3 ns to 200 ms	2 ns to 200 ms variable	0.8 ns or 1.6 ns selectable
Minimum	variable		
(with overprogramming)	≤ 3 ns	≤ 2ns/1.4 ns typ. For ELC levels (20/80) 5 ns typ. For 1 KΩ source impeded	≤ 600 ps for Vpp ≤ 1 V 450 ps typ. For ELC levels (20/80) ≤ 900 ps for Vpp > 1 V
Accuracy	± 10% ± 200 ps typ. ; ± 10% ± 400 ps		
Linearity	3% typ. For transitions > 100 ns		N/A

Burst Count: 2 to 65536 (single or double pulses).

Delay: delay, phase or % of period.

Double pulse and delay: mutually exclusive.

Duty cycle: set between 0.1% and 95% (subject to width limits.
99.9% with overprogramming).

Repeatability: is typ. four times better than accuracy.

Transition times: leading/ trailing edge or % of width. Leading and trailing edges are independent Agilent 81111A/Agilent 81105A) within one of the following overlapping segments (1:20 ratio): 2 ns (3 ns) - 20 ns, 10 ns - 200 ns, 100 ns - 2 ms, 1µs - 20 µs, 10 µs - 200 µs, 100 µs - 2 ms, 1 ms - 20 ms, 10 ms - 200 ms.

Output timing fidelity: period, delay and width are continuously variable without any output glitches or dropouts.

Overprogramming: all parameters of the Agilent 81110A, except transitions, can be set to whatever the 330 MHz timing system will allow. This applies also when the Agilent 81111A (165 MHz) output module is used.

Level/Pulse Performance Characteristics

Level specifications are valid after a 5 ns (Agilent 81112A) or 30 ns (Agilent 81111A/Agilent 81105A) typical settling time.

Mainframe		Agilent 81101A Agilent 81105A	Agilent 81110A Agilent 81111A	Agilent 81110A Agilent 81112A
Amplitude	50 Ω into 50 Ω	100 mV$_{pp}$ to 10.0 V$_{pp}$		100 mV$_{pp}$ to 3.8 V$_{pp}$
Level window	50 Ω into 50 Ω	-10.0 V to +10.0 V		- 2.0 V to 3.8 V
	1 kΩ into 50 Ω	-20.0 V to +20.0 V		N/A
Accuracy	50 Ω into 50 Ω	± (3% + 75 mV)	± (1% + 50 mV)	± (2% + 50 mV)
	1 kΩ into 50 Ω	± (3% + 150 mV) [1]	± (1% + 100 mV)[1]	N/A
Resolution	50 Ω into 50 Ω	10 mV		10 mV
	1 kΩ into 50 Ω	20 mV		N/A
Output connectors		BNC single-ended		BNC differential
Source Impedance		Selectable 50 Ω or 1 kΩ		50 Ω only
	Accuracy	Typ. ± 1%		
Max. external voltage		± 24 V		-2.2 V to +5.5 V
Short circuit current		±400 mA max. (doubles for channel addition)		-84 mA to + 152 mA
Dynamic Crosstalk		< 0.1% typ.		
Base line noise		10 mV RMS typ. 4 mV RMS typ.		
Overshoot/preshoot/ringing		± 5% of amplitude ± 20 mV		± 5% of amplitude ± 50 mV

Note:
(1) in ± 19 V level window

Level parameters: voltage or current, high or low level, offset or amplitude.

On/off: relays connect/ disconnect output (HiZ)

Load compensation: the actual load value can be entered (for loads ≠ 50 Ω) to display actual output values.

(Applies to the Agilent 81105A and Agilent 81111A only).

Normal/complement: selectable.

Limit: programmable high and low levels can be limited to protect the device-under-test.

Channel Addition (with Agilent 81105A or Agilent 81111A output channels)

If the instrument is equipped with 2 output modules, channel 2 can be added to channel 1 internally. In this case the second output is disabled. The additional fixed delay on the second channel is typ. 2.5 ns. The following parameters differ from the above specifications if two output modules (Agilent 81105A/Agilent 81111A) are added.

Mainframe		Agilent 81104A with two Agilent 81105A output modules	Agilent 81110A with two Agilent 81111A output modules
Amplitude	50 Ω into 50 Ω	100 mVpp tp 20.0 Vpp	
	1 kΩ into 50 Ω	200 mVpp to 20.0 Vpp	
Source Impedance		Selectable from 50 Ω or 1 kΩ	
Level window	50 Ω into 50 Ω	-20.0 V +20.0 V	
	1 kΩ into 50 Ω	-20.0 V to +20.0 V	
Max. frequency	50 Ω channel	60 MHz typ.	
	1 kΩ channel	15 MHz typ.	
Min. transitions	50 Ω channel	2 ns typ. (channel one) 5 ns typ. (channel two)	
	1 kΩ channel	20 ns typ. both channels	

Pattern Mode

Pattern length: 16 kbit/channel and strobe output.

Output format: RZ (return to zero), NRZ (non-return to zero), DNRZ (delayed non-return to zero).

Random pattern:
PRBS $2^{(n-1)}$ n = 7,8,...,14.

Trigger Modes

Continuous: continuous pulses, double pulses, bursts (single or double pulses) or patterns.

External triggered: each active input transition (rising, falling or both)
generates a single or double pulse, burst or pattern.

External gated: the active input level (high or low) enables pulses, double pulses, bursts or patterns. The last single/double pulse, burst or pattern is always completed.

External width: the pulse shape can be recovered. Period and width of an external input signal is maintained. Delay, levels and transitions can be set.

Manual: simulates an external input signal.

Internal triggered: internal PLL replaces an external trigger source. Pulses, double pulses, bursts or patterns can be set.

Inputs and Outputs

Clock input/PLL reference and external input

PLL reference: (BNC connector at rear panel). The internal PLL is
locked to an external 5 MHz or 10 MHz reference frequency.

Clock input: (BNC connector at rear panel). The output period is determined by the signal at CLK input.

Ext. input: used for trigger, gate or external width.

Input impedance:
50 Ω/10 kΩ selectable.

Threshold: - 10 V to + 10 V.

Max. input voltage: ± 15 Vpp.

Sensitivity: ≤ 300 mVpp typical.

Transitions: < 100 ns.

Frequency: dc to max. frequency of output module.

Min. pulsewidth: 1.5 ns (as width of output module in external width mode).

Strobe output and trigger output

Strobe output: user-defined, 16 kbit pattern (NRZ) when in pattern mode.

Trigger format: one pulse per period with 50% duty cycle typical. External mode: 1.5 ns typ. for Agilent 81110A. 5.9 ns typ. for Agilent 81104A.

Level: TTL or ECL selectable.

Output impedance: 50 Ω typical.

Max. external voltage: - 2 V/+7 V.

Transition times: 1.0 ns typical for TTL, 600 ps typical for ECL.

Typical delay (Agilent 81110A with Agilent 81111A output module) [1]

Instrument mode	From	To	Typ. value
External width	Ext. Input	Strobe/Trigger out	8.5 ns
		Output 1/Output 2	19.5 ns
All other modes	Ext. Input/Clk Input	Strobe/Trigger out	12.0 ns
		Output 1/Output 2	26.0 ns
	Strobe/Trigger out	Output 1/Output 2	14.0 ns

Note:
[1] Subtract 4 ns from the typ. delay value when referring to OUTPUT1/2 for the Agilent 81112A output module and add 1 ns when referring to OUTPUT1/2 for the Agilent 81104A with the Agilent 81105A output module.

81130A Specifications

Timing Characteristics

Measured at 50% amplitude at fastest transitions in continuous mode and 50 Ω source impedance. The Agilent 81130A is designed and recommended for an operation in the frequency range of 170 kHz to 400/660 MHz. However it can be operated in the extended range down to 1 kHz. Changes in specifications below 170 kHz are marked.

Mainframe Output module	Agilent 81130A Agilent 81131A	Agilent 81130A Agilent 81132A
Frequency range	170 kHz (1 kHz) to 400 MHz	170 kHz (1 kHz) to 660 MHz
Frequency resolution	4 digits, (2 ps best case)	
Period Range	2.5 ns to 5.9 µs 1.50 ns to 5.9 µs (f < 170 kHz: 2.5 ns to 1 ms)	(f < 170 kHz: 1.5 ns to 1.0 ms)
Accuracy	± 100 ppm	
RMS jitter (int ref, int clk)	0.001% + 15 ps	
Width range	1.25 ns to period - 1.25 ns)	1.25 ns to period - 1.25 ns)
Width resolution	4 digits (2 ps best case) (f < 170 kHz: 0.05% of period)	
Width accuracy	± (100 ppm + 200 ps) (f < 170 kHz: 0.06% of period)	
Width jitter	0.001% + 15 ps	
Add, variable delay range	0 to 3.00 µs independent of period (> 3 µs: one to 1 period)	
Delay resolution	4 digits (2 ps best case) (f < 170 kHz: ± 0.05% of period)	
Delay accuracy	± (0.01% + 100 ps) relative to zero delay (f < 170 kHz: ± 0.035% of period)	
Delay jitter	0.001% + 15 ps	
Fixed delay (clk in to out)	53 ns	
(ext. in to out)	54 ns + 0 to 1 period (1)	
Transition time range (10/90)	800 ps or 1600 ps	fixed
Minimum transition (10/90)	≤ 600 ps for Vpp ≤ 1 V ≤ 900 ps for Vpp ≤ 1 V	500 ps typ.
At ELC levels (20/80)	450 ps typ.	< 350 ps (200 ps typ.)
Deskew range	± 25 ns	

Note:
(1) The uncertainty of 1 period can be eliminated if an external clock and the following setup and hold times are upheld.
setup time: 0.3 ns to 4.3 ns; hold time: -2.8 ns to 4.0 ns.

Burst Count: 2 to 65504.

Delay: delay, phase or % of period.

Duty cycle: set between 0.1% and 99,9% (subject to width limits).

Repeatability: is typ. four times better than accuracy.

Level/Pulse Performance Characteristics

Level specifications are valid after a 30 ns typical settling time (50 Ω into 50 Ω terminated to ground).

Mainframe	81130A	81130A
Output module	81131A (400 MHz)	81132 A (660 MHz)
Amplitude	0.10 Vpp to 3.80 Vpp	0.10 Vpp to 2.50 Vpp
Level Window	-2.00 V to +3.80 V	-2 .00 V to +3.00 V
Accuracy	± (5% +150 mV)	
Resolution	3 digits (10 mV best case)	
Output Impedance	50 Ω ± 1%typ.	50 Ω ±5%typ.
Max. external voltage	- 2.2 to +5.5V	-2.0 to +4.0 V
Short circuit current	-80 mA to +152 mA.	-80 mA to +120 mA
Baseline noise	4 mV RMS typ.	8 mV RMS typ.
Overshoot/preshoot/ringing	±(5% + 50 mV) of amplitude typ.	±(5% + 100 mV) of amplitude typ.

Level parameters: Voltage or current, high and low level, or offset and amplitude.

Pattern and Sequencing

Pattern length: 65504 bit/channel. If PRBS is used: (65503-RBLength)

Pattern formats: NRZ (non-return-to-zero), DNRZ (delayed non-return-to-zero), RZ (return-to-zero) and R1 (return-to-one) can be selected (see figure 1)

On/off: Relays connect/disconnect output (HiZ).

Sequencing: A sequence is a succession of segments. One outer loop running once or continuous, and one nested loop can be applied. The nested loop can be set from 1 to 2^{20} repetitions.

Segment: The memory can be divided into maximal 4 segments.

Segment length resolution: This is the resolution for which the segment can be set dependent on the maximum data rate. (see table 1)

Limit: Programmable high and low levels can be limited to protect the device-under-test.

Segment types: Pattern, PRBS, high and low segments ("0" or "1" levels segments selectable). Note: If one channel is set to PRBS the other channel can only be high or low segments, or PRBS type.

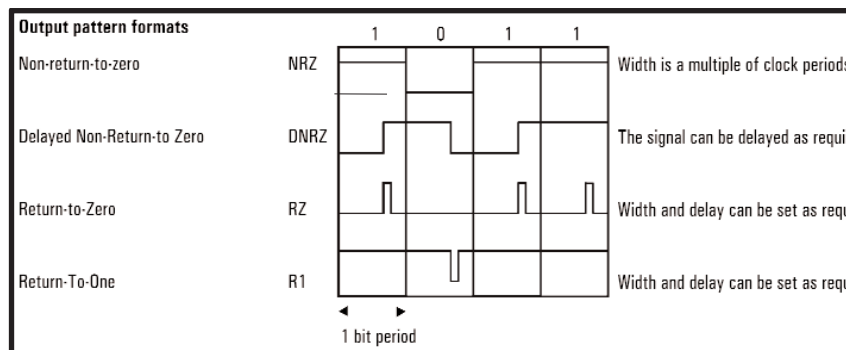**Random Pattern:** PRBS 2^n-1, n = 7,8,...,15 (CCITT 0.151)

Figure 1: Pattern Formats

Required Segment length resolution [1]	Maximum data rate, Mbit/s
1 bit	41.67
2 bits	83.88
4 bits	166.67
8 bits	333.33
16 bits	660

Table 1 . Segment length resolution trade-offs

[1] **The minimum length in the first segment of a nested loop is two times that of the segment length resolution.**

Digital Channel Addition

Channel 1 can be logically combined with channel 2 (XOR) as shown in Figure 2. The source impedance remains 50 Ω. Output 2 is still available in this case.
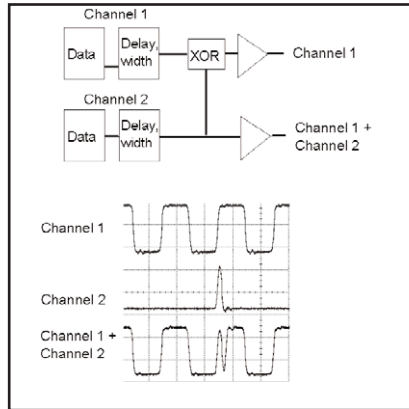

Figure 2: Channel addition

Trigger Modes

Continuous: Continuous pulses, bursts or patterns.

External started: Each active input transition (rising, falling edge) generates pulses, bursts or patterns.

External gated: The active input level (high or low) enables pulses, bursts or patterns. On an external gate signal the output is immediately stopped, that means the last cycle will not be completed.

Manual: Simulates an external input signal with push of a front panel button.

Inputs and Outputs

Clock input/PLL reference and external input

Connectors: SMA (f) 3.5 mm
Input impedance: 50 Ω
Termination voltage: -2.10 V to 3.30 V
Input sensitivity: < 400 mV typ.
Max. Input Voltage: -3 V to + 6 V
Input transitions: < 20 ns

Only valid for clock input/PLL reference One input is used for clock input or for the PLL reference alternatively.

Reference: The internal PLL is locked to the 1,2,5 or 10 MHz.

External clock: The output period is determined by the signal at clock input.

Clock Input frequency: 170 kHz to 660 MHz (at 50% ±10% duty cycle)

Delay from input trigger output: 21ns.

Delay from input to output: 53ns

Threshold: ac coupled

Only valid for external input

External input: Used for external started or gated

Input frequency: DC to 330MHz

Delay from external input to trigger output: 22ns + 0 to 1 period

Delay from external input to output: 54 ns + 0 to 1 period

Threshold: -1.4 V to +3.7 V

Trigger output

Trigger format: One pulse per period with 50% duty cycle typical. In pattern mode the trigger pulse can be set to mark the start of any segment.

Output impedance: 50 Ω typical.

Level: TTL/ETTL (for frequency < 180 MHz), 1 V to GND, ECL 50 Ω to GND/-2 V, PECL 50 Ω to + 3 V.

Max. external voltage: -2 V/+3 V.

Transition times: 1.0 ns typical for TTL, 600 ps typical for ECL.

Delay from external input to trigger output: 32 ns typical

Programming times: (measured at display off.)

ASCII Command	Typical execution time
Width, delay, transition times	40 ms to 70 ms
Period within one range [1]	100 ms to 260 ms
Period between different ranges [1]:	
In pulse/burst mode	140 ms to 300 ms
in pattern mode	100 ms to 5.05 s
Levels	43 ms
Trigger modes	< 75 ms
Input parameters	28 ms
Save setting	200 ms
Recall setting:	
a) in pulse/burst mode	515 ms to 800 ms
b) in pattern mode with data	1.15 s to 5.5 s
and PRBS (depends on setting)	
65504 bit pattern transfer	1.25 s
Pattern and sequencing (depends on setting)	190 ms to 5.1 s

[1] Range depends on segment length resolution, see table 1

Common Specifications

User Interface

Overprogramming: all parameters can be overprogrammed (exceeding specifications) to fully exploit the hardware limits.

Setting check: warning messages indicate potentially conflicting parameters due to inaccuracy. Error messages indicate conflicting parameters.

Help key: displays a context-sensitive message.

Autoset key: resolves all timing conflicts.

Non-volatile memory: current setting is saved on power-down. Up to nine user settings and one fixed default setting can be stored in the instrument.

Memory card: 99 settings can be stored on a 1 MB PCMCIA card (MS-DOS®).

Remote Control
Operates according to IEEE standard 488.2, 1987 and SCPI 1992.0.
Function Code: SH1, AH1, T6, L4, SR1, RL1, PP0, DC1, DT1, C0.

ASCII command	Typ. exec. time
One parameter or mode	30 ms typ.
Recall setting	250 ms typ.
16 k pattern transfer	600 ms typ.

Programming times: All checks and display off.

Specifications

Specifications describe the instrument's warranted performance. Non-warranted values are described as typical. All specifications apply after a 30 minute warm-up phase with 50 Ω source/load resistance. All specifications are valid from 0°C to 55°C ambient temperature.

General

Operating temperature:
0°C to +55°C.

Storage temperature:
-40°C to +70°C.

Humidity: 95% r.h. up to 40°C ambient temperature.

EMC: conforms to EN50082-1, EN 55011, Class A.

Noise emission: 5.7 bel typical.

Battery: Lithium CR2477-N.

Safety: IEC1010, CSA1010.

Power requirements:
100-240 Vac, ± 10%, 50-60 Hz;
100-120 Vac, ± 10%, 400 Hz.

Power consumption:
300 VA max.

Max. dimensions (H * W * D):
89 mm * 426 mm * 521 mm.

Weight: 9.2 kg net, 13.8 kg shipping.

Recalibration period:
Three years recommended.

Complementary Products
Pulse Pattern Generator and Oscilloscopes (Real Time or Sampling)
DSO 80804B/80604B
DSO 80404B
DSO 80304B
D/MSO 6100/8104A
D/MSO 6050/8064A
D/MSO6030
D/MSO 601x, DSO 3000

Inputs and Outputs

Clock input/PLL reference and external input

Connectors: SMA (f) 3.5 mm

Input impedance: 50 Ω

Termination voltage: –2.10 V to 3.30 V

Input sensitivity: < 400 mV typ.
Max. Input Voltage: –3 V to + 6 V

Input transitions: < 20 ns

Only valid for clock input/PLL reference
One input is used for clock input or for the PLL reference alternatively.

Reference: The internal PLL is locked to the 1,2,5 or 10 MHz .

External clock: The output period is determined by the signal at clock input .

Clock Input frequency: 170 kHz to 660 MHz (at 50% –10% duty cycle)

Delay from input trigger output: 21ns.

Delay from input to output: 53ns

Threshold: ac coupled
Only valid for external input

External input: Used for external started or gated

Input frequency: DC to 330MHz

Delay from external input to trigger output: 22ns + 0 to 1 period

Delay from external input to output:

Ordering Information - 81100 Family

The minimum configuration for a working instrument consists of a mainframe and one output module. The second output module can be added later. Output modules can be exchanged and retrofitted by the user. The Reference Guide (811xx-91021) is supplied with each mainframe for all configurations. A memory card is not included.

Each Agilent 81101A mainframe includes one output channel (in comparison to the other models of the Agilent 81100 family). The output module of the 81101A does not need to be ordered separately.

Agilent 81101A 50 MHz one channel Pulse Generator, 10V

Quick Start Guide language options
Opt OBI Engish Guide
 (811xx-91021**)**
Opt ABF French Guide
 (81101-91210)
Opt ABJ Japanese Guide
 (81101-91510)
Opt AB0 Taiwan Chinese Guide
 (81101-91610)
Opt AB1 Korean Guide
 (81101-91710)
Opt AB2 Chinese Guide
 (81101-91810)

Additional documentation options
Opt 0BW Service Manual
 (81101-91021)

Agilent 81104A
80 MHz Pulse/Pattern Generator Mainframe
Output module:
Agilent 81105A   80 MHz, 10 V

Agilent 81110A
330/165 MHz Pulse/Pattern Generator Mainframe
Output modules:
Agilent 81111A   165 MHz, 10 V
Agilent 81112A   330 MHz, 3.8 V

Note: Only use output modules of the same module number. A combination of the Agilent 81111A and Agilent 81112A in one Agilent 81110A is not possible.

Quick Start Guide language options
Opt OBI   Engish Guide
 (811xx-91021**)**
Opt ABF   French Guide
 (81110-91210)
Opt ABJ Japanese Guide
 (81110-91510)
Opt AB0   Taiwan Chinese Guide
 (81110-91610)
Opt AB1   Korean Guide
 (81110-91710)
Opt AB2   Chinese Guide
 (81110-91810)

Additional documentation options
Opt 0BW   Service Manual
 (81110-91021)

Agilent 81130A
400/660 MHz Pulse/Data Generator Mainframe
Output modules:
Agilent 81131A   400 MHz, 3.8 V
Agilent 81132A   660 MHz, 2.4 V

Note: Only use output modules of the same module number. A combination of the Agilent 81131A and Agilent 81132A in one Agilent 81130A is not possible.

Quick Start Guide language options
Opt OBI   Engish Guide
 (811xx-91021**)**
Opt ABF   French Guide
 (81130-91220)
Opt ABJ Japanese Guide
 (81130-91520)
Opt AB0   Taiwan Chinese Guide
 (81130-91620)
Opt AB1   Korean Guide
 (81130-91720)
Opt AB2 Chinese Guide
 (81130-91820)

Additional documentation options
Opt 0BW Service Manual
 (81130-91021)
Opt 0B1 English Quick Start
 Guide (includes English
 Referemce Guide)
Opt ABJ Japanese Quick Start
 Guide (includes English
 Referecnce Guide)
Opt 0B0 Does not include any
 Quick Start Guide
 (includes EnglishReference
 Guide)

All options are orderable with the mainframes.

Accessories
Opt UN2 Rear Panel Connectors (instead of front
 panel)
Opt 1CP Rack Mount and Handle Kit (5063-9219)
Opt 1CN Handle Kit (5063-9226)
Opt 1CM Rack Mount Kit (5063-9212)
Opt 1CR Rack Slide Kit (1494-0059)
Opt UFJ 1 MB SRAM Memory Card (0950-3380)
Opt UK6 Commercial cal. certificate with Test
 Data

Related Agilent Literature	Pub.No.
Agilent Family of Pulse/Pattern Generators, Brochure	**5980-0489E**
Radar Distance test to airborne planes Application Note	**5968-5843E**
The Dual Clock Gbit Chip test Application Note	**5968-5844E**

For more information, please visit us at
www.agilent.com/find/pulse_generator

Product specifications and descriptions in this document subject to change without notice.

For the latest version of this document, please visit our website at
www.agilent.com/find/pulse_generator
and go to the Key Library Information area or insert the publication number
(**5980-1215E**) into the search engine.

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Phone or Fax

United States:
(tel) 800 829 4444
(fax) 800 829 4433

Canada:
(tel) 877 894 4414
(fax) 800 746 4866

China:
(tel) 800 810 0189
(fax) 800 820 2816

Europe:
(tel) 31 20 547 2111

Japan:
(tel) (81) 426 56 7832
(fax) (81) 426 56 7840

Korea:
(tel) (080) 769 0800
(fax) (080)769 0900

Latin America:
(tel) (305) 269 7500

Taiwan:
(tel) 0800 047 866
(fax) 0800 286 331

Other Asia Pacific Countries:
(tel) (65) 6375 8100
(fax) (65) 6755 0042
Email: tm_ap@agilent.com
Revised: 09/14/06

Product specifications and descriptions in this document subject to change without notice.

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Printed in the USA, October 5th 2006

5980-1215E

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